Ronald Mraz Ph.D.

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**Curriculum Vitae**

My teaching interests center on Cyber-Security, High Performance Computing (HPC), Computational Science, Computer Architecture, Computer Organization, Software Engineering and Operating Systems. Additionally, I am interested in distributed computing, critical infrastructure controls, smart grid operation, entrepreneurship and computer network security.

My research interests include HPC Computational Science, Smart Grid Infrastructure, High Performance Supercomputing Architectures, Message Passing Interfaces, Distributed Systems, Shared Memory Architectures, Operating System Interference of HPC, Control Theory, and Information Assurance.

**Education**

**Ph.D. Electrical and Computer Engineering, Carnegie Mellon University 1992**, Pittsburgh, PA. Thesis topic: “*A RISC-Based Architecture for Real-Time Computation”*. Thesis Committee: Jay K. Strosnider, John P. Shen, Zary Segall and Gabriel Silberman.

**M.Sc. Electrical Engineering, Syracuse University**, Syracuse, NY.

**B.Sc. Electrical Engineering, Drexel University**, Philadelphia, PA.

**Academic Employment**

**US Coast Guard Academy (USCGA), Full-Time Lecturer**. New London, CT. Fall 2018 to 2020. Department of Electrical Engineering and Cyber Systems.Undergraduate level Instruction.

* **Introduction to Information Security.** Course Coordinator in the new formed Cyber Systems major at USCGA. Overview and introduction to the Cyber Security Landscape. Including HW/SW system vulnerabilities, law enforcement, encryption, authentication, confidentiality, availability and attacks. (2nd year class)
* **Software Engineering with Lab.** C# Object Oriented programming with SQL operations culminating in cadets proposing and implementing a software product within an Agile Team project. (3rd year class.)
* **Introduction to Computing** STEM computing class studying algorithms, advanced Excel functionality and MATLAB programming. Skills learned here will be required for upper level STEM classes. (1st year class.)
* **Capstone Advisor** Advising an interdisciplinary team of students to create an Autonomous Surface Vehicle (ASV) that performs tasks relevant to the Coast Guard Missions. (4rd year class.)
* **Independent Study** Supervision of undergraduate research in AI Image Processing for US Coast Guard related applications. (3rd year class.)

**The University at Albany (SUNY), Adjunct Professor**. Albany, NY. Fall 2017 and Spring 2018, Computer Science Department. Graduate level instruction.

* **Computer Organization.** Assembly language compilation optimization, design and operation of synchronization primitives, parallel computation implications to memory hierarchy and deadlock considerations. (Graduate Level)
* **Operating Systems with Lab,** Operating system design and architecture, user interface library design with processes and threads, abstraction of synchronization primitives, deadlock and live lock analysis, memory hierarchy abstraction, storage architecture and design, multiprocessor system support. (Graduate Level)

**Academic Service**

**Cyber Council**. US Coast Guard Academy, New London, CT. Member. Writing of grant proposals for DOD funding and support for academic infrastructure for the new Cyber Systems offering. Most recent being DOD Grants for Institutional Capacity Building to provide equipment for an Experimental Cyber-Physical Lab. 2018-2020.

**New York Institute of Technology**. New York, NY. Member of the Academic Advisory Board, School of Engineering and Computer Sciences (SoECS). Dr. Nada Anid, Dean and Chairman. Participated in the Technology Inter-Operability Standing Committee on initiatives for student enrichment including renewing ABET accreditation. 2014-2019.

**Workshop on Operating System Interference in High Performance Applications** - OSIHPA **2005, OSIHPA 2006** Held with the 14th/15th International Conference on Parallel Architectures and Compilation Techniques. Co-organizer. <http://osihpa.cs.utep.edu/2005/cfp.html> and <http://osihpa.cs.utep.edu/>

**Industry Employment**

**Owl Computing Technologies, Inc.** Board Chairman, President, CEO, CTO and Founder. (Now Owl Cyber Defense Solutions, LLC, a DC Capital Partners portfolio company) Owl Computing markets and sells special purpose internet firewalls with the security policies enforced by a hybrid HW/SW system. The company was started by licensing a concept patent from Sandia National Labs and developing a marketable product. In doing so, the company pioneered the data-diode security market by evolving the technology to a scalable appliance for cyber security. The technology used in all products is certified by the National Information Assurance Partnership (NIAP). At the time of acquisition in 2017, by DC Capital Partners, the Company has grown to a global concern of 50+ employees. I then provided corporate transition leadership and guidance for the acquisition of Owl Computing Technologies, Inc. 1998- April 2017.

**IBM Research, Hawthorne, NY.** Research Staff Member. As an RSM Scientist I researched, High Performance Computing (HPC) Architectures and Message Passing System interfaces for shared memory (PVS and AS/400) and distributed memory systems (RP3 and Vulcan). These message passing systems were validated with established benchmarks for molecular dynamics modelling, automobile crash simulations, FFT for oil exploration, weather modelling and an enhanced database system (IBM DB2) for parallel operation on HPC systems. Partnered with Argonne National Labs for a scalable media server incorporating a zero-copy I/O interface or ZATM. Implemented the reference designs for database system parallelization of DB2 and for RTSP, a real-time streaming video control protocol. (RFC 2326) Developed a hybrid hardware/software backup system accelerator for Tivoli Backup System. Researched TCP/IP offload accelerators. 1992-2005.

**IBM Resident Study Fellowship,** Carnegie Mellon University, Pittsburgh, PA. enrolled in the Computer Engineering department. Research Staff Engineer. Was awarded a Ph.D. in Electrical and Computer Engineering and returned to IBM Research as a Research Staff Member. 1989-1992.

**IBM Research, Yorktown Heights, NY.** Research Staff Engineer. As an Engineer, I developed custom RISC based systems for empirical experiments of HPC message passing architectures such as RP3 and Vulcan. An Instructor for an IBM Internal Classes. *“High Performance Computer Architecture.”* Awarded an IBM Resident Study Fellowship to CMU in 1989. 1984-1989.

**IBM Server Division, Poughkeepsie, NY.** Senior Associate Engineer. As an engineer, designed memory systems for high performance mainframe array and vector processors for attached and stand-alone systems. 1982-1984.

**Westinghouse Research. Pittsburgh, PA**. Engineer. Modeled induction motor designs in computer simulations to optimize feedback parameters for digital controls. Designed computer controllers for switching power convertors for induction motor drives, VAR compensators as well as researched controller requirements for alternative energy sources such as solar arrays, wind, fuel cells and magneto-hydrodynamics. 1980-1982.

**Publications**

Mraz, R., Kessler G. C., Gold, E., and Cline, J. G. “**Enhanced Iceberg Information Dissemination for Public and Autonomous Maritime Use**,” in World Academy of Science and Technology, International Journal of Transport and Vehicle Engineering, Vol: 14, No. 4, 2020.

I.J. Davis, R.C. Holt, R. Mraz “**Fact extraction from bash in support of script migration**,” in Software Evolution Week - IEEE Conference on Software Maintenance, Reengineering, and Reverse Engineering(CSMR-WCRE), 2014, Pages: 363 – 366. (Owl funded research at Univ. of Waterloo)

J. Menoher, R. Mraz “**Secure Cross Border Information Sharing Using One-Way Data Transfer Systems**”, Presented at ISGIG, the International Symposium on Global Information Governancein Pisa, Italy. 2009.

J. Menoher, R. Mraz “**Coalition Warrior Interoperability Demo (CWID) 2007 Data Diode Case Study”,** InvitedAnnual Computer Security Applications Conference (ACSAC), 2007 Presentation.

J. Menoher, J. Hope, A. Holmes, R. Cooper, R. Mraz “**Transferring Large files in Real-Time**”, Presented at the 2nd Int’l Workshop on Operating System Interference in High Performance Applications (OSIHPA), 2006. In conjunction with PACT-06.

D Freimuth, E. Hu, J. LaVoie, R. Mraz, E. Nahum, J. Tracey “**Evaluating Batching for TCP Offload**” in RC23894 of IBM Research Reports, 2005

D Freimuth, E. Hu, J. LaVoie, R. Mraz, E. Nahum, J. Tracey “**Server Network Scalability and TCP Offload**,” in USENIX Annual Technical Conference, 2005, Pages 209 – 222.

 A.K.Iyengar, R. Mraz, M.E. Zurko “**Performance Considerations in Web** Security,” Chapter in Certification and Security in E-Services. IFIP – The International Federation for Information Processing, vol 127. 2002, Pages 57-71, Springer, Boston, MA.

R. Mraz, K Witting, P.M. Dantzig “**Using SSL Session ID Reuse for Characterization of Scalable Secure Web Servers**”, Tec**h**nical Report RC 22323(Revised May 5, 2002), IBM Research Division, Yorktown Heights, NY, September 2002.

R. Mraz “**Secure Blue: an architecture for a scalable, reliable high-volume SSL Internet server,”** in the Annual Computer Security Applications Conference (ACSAC) Year: 2001, New Orleans, Louisiana, 2001.

J. Yin, M. Yousif, R. Mraz. "**Improving the Performance of the Tivoli Storage Manager with Threaded Hardware Compression**" in RC21808 of IBM Research Reports

R. Mraz, E Nowicki, M Thoennes “**A high performance Get-Put interface for ATM communications**”, In Proceedings of the Centre for Advanced Studies Conference (CASCON),1998.

R. Mraz "**A Methodology for Performance Analysis Using System Event Plots**" in RC21281 of IBM Research Reports

D. Freimuth, R. Auerbach, R. Mraz, E. Nowicki, D. Zumbo, M. Ritter (1997). "**A Common Data Link Interface for a Prototype ATM Adapter**" in RC20891 of IBM Research Reports

L. Womack, R. Mraz, A. Mendelson “**A study of virtual memory MTU reassembly within the PowerPC architecture,”** in Proceedings of the IEEE Fifth International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS),1997, Pages: 81 – 90.

R. Mraz, D. Freimuth, E. Nowicki and G. Silberman. "**Using Commodity Networks for Distributed Computing Research**" in RC20445 of IBM Research Reports (1996)

R. Mraz "**Reducing the variance of point-to-point transfers for parallel real-time programs**," inIEEE Parallel & Distributed Technology: Systems & Applications**,** vol. 2, no. 4, pp. 20-31, Winter 1994.

R. Mraz “**Reducing the variance of point to point transfers in the IBM 9076 parallel computer**, “in Supercomputing '94: Proceedings of the 1994 ACM/IEEE Conference on Supercomputing, 1994, Pages: 620 – 629.

R. Mraz “**The Effect of Operating System Scheduling on High Performance Message Passing Parallel Systems**” in Proceedings of the 7th Intl Conf on Parallel and Distributed Computing Systems (PDCS ’94) Las Vegas, Nevada 1994, Pages: 100 – 104. (IDA Gov’t Contract)

R. Mraz “**EUIm: A message passing library for the IBM power visualization system**,” in Proceedings of the IEEE Workshop on Advances in Parallel and Distributed Systems, 1993, Pages: 53 – 58. (IDA Gov’t Contract)

R. Mraz. **A RISC Based Architecture for Real-Time Computation**. Ph.D. thesis, Carnegie Mellon University, May 1992available athttps://www.ece.cmu.edu/research/publications/1992/CMU-ECE-1992-070.pdf

R. Mraz, G. Palmer, J.K. Strosnider “**Analysis of architectures for fault-tolerant computation**,” in the Proceedings of theIEEE Twenty-Fourth Annual Hawaii International Conference on System Sciences, Year: 1991, Pages: 334 - 343 vol.1.

 R. Mraz, M. White, J.K. Strosnider “**A methodology to evaluate architectures for real-time control**,” in the IEEE International Conference on Systems Engineering, 1990 Pages: 449 - 453,

**Awards and Professional Associations**

**CT Quality Innovation Awards** in 2009 and 2010. Multiple awards to Owl Computing Technologies in quantified improvement of corporate processes. Award recognition is based on the Malcolm Baldrige criteria.

Awarded an **IBM Resident Study Fellowship** to Carnegie Mellon University for Ph.D. studies. This included paid tuition, expenses and salary for 3 years. 1989-1991.

Multiple **Patent Innovation awards** at IBM Research, including patent plateau achievement awards in March 1997, June 2001 and October 2003.

**IBM Corporate Innovation Award** for patent application on distributed shared memory.

**Research Division Technical Group** **Award** for Contributions to the Multi-Point Video Access and Conferencing System at 1996 Summer Olympics.

**Research Division Technical Group Award** for Contributions to the Deep Blue Chess Computer in the ACM Chess Challenge

**Research Division Technical Group Award** for Contributions to the External User Interface Library (EUIm lib)

**IBM Research Division** **Award** for the development of auxiliary tools for the logic design of the Research Parallel Processor.

Senior Member of Institute of Electrical and Electronic Engineers. (IEEE)

Member of Association of Computing Machinery. (ACM)

**Patents**

Sorted by subject area. Additional published, domestic and international applications in process.

* **High Performance Supercomputing Architectures**

U.S. Patent # 5,802,288 “Integrated communications for pipelined computers”

* **Operating Systems**

U.S. Patent # 9,736,121 “File manifest filter for unidirectional transfer of files”

U.S. Patent # 9,436,825 “System and method for integrity assurance of partial data”

U.S. Patent # 6,829,764 “System and method for maximizing usage of computer resources in scheduling of application tasks”

U.S. Patent # 6,516,342 “Method and apparatus for extending memory using a memory server”

U.S. Patent # 5,930,830 “System and method for concatenating discontinuous memory pages”

U.S. Patent # 5,701,446 “Method for fine grain adjustments to system time in computer systems”

* **Message Passing Interfaces, Distributed Systems, Networking**

U.S. Patent # 8,392,827 “Method for generation and assembly of web page content”

U.S. Patent # 8,332,531 “Supporting memory management in an offload of network protocol processing”

U.S. Patent # 8,316,109 “Supporting memory management in an offload of network protocol processing”

U.S. Patent # 7,962,628 “Apparatus and method for supporting connection establishment in an offload of network protocol processing”

U.S. Patent # 7,930,422 “Apparatus and method for supporting memory management in an offload of network protocol processing”

U.S. Patent # 7,533,176 “Method for supporting connection establishment in an offload of network protocol processing”

U.S. Patent # 7,493,427 “Apparatus and method for supporting received data processing in an offload of network protocol processing”

U.S. Patent # 7,114,096 “State recovery and failover of intelligent network adapters”

U.S. Patent # 7,085,923 “High volume secure internet server”

U.S. Patent # 6,968,358 “Method and apparatus for network communication card memory management”

U.S. Patent # 6,526,434 “System and method for efficient transfer of data blocks from client to server”

U.S. Patent # 5,544,162 “IP bridge for parallel machines”

WO 2006046972 A1 “Apparatus and method for supporting memory management in an offload of network protocol processing”

CA 2573156 C “Apparatus and method for supporting memory management in an offload of network protocol processing”

* **Information Assurance**

U.S. Patent #9,894,083 “System for providing a secure video display”

U.S. Patent #9,880,869 “Single computer-based virtual cross-domain solutions”

U.S. Patent # 9,853,918 “One-way network interface”

U.S. Patent # 9,712,543 “System for remotely monitoring status information of devices”

U.S. Patent # 9,680,794 “Secure one-way interface for Archestra data transfer”

U.S. Patent # 9,678,921 “Method and apparatus for data transfer reconciliation”

U.S. Patent # 9,641,499 “One-way interface for PI to PI data transfer “

U.S. Patent # 9,596,245 “Secure one-way interface for a network device”

U.S. Patent # 9,575,987 “System and method for providing assured database updates via a one-way data link”

U.S. Patent # 9,380,064 “System and method for improving the resiliency of websites and web services”

U.S. Patent # 9,380,023 “Enterprise cross-domain solution having configurable data filters”

U.S. Patent # 9,311,329 “System and method for modular and continuous data assurance”

U.S. Patent # 9,306,953 “System and method for secure unidirectional transfer of commands to control equipment”

U.S. Patent # 9,305,189 “Ruggedized, compact and integrated one-way controlled interface to enforce confidentiality of a secure enclave”

U.S. Patent # 9,282,102 “Secure front-end interface”

U.S. Patent # 9,094,401 “Secure front-end interface”

U.S. Patent # 9,088,558 “Secure one-way interface for OPC data transfer”

U.S. Patent # 9,088,539 “Data transfer system”

U.S. Patent # 9,081,520 “Remote print file transfer and spooling application for use with a one-way data link”

U.S. Patent # 9,065,878 “System and method for providing a remote virtual screen view”

U.S. Patent # 8,997,202 “System for secure transfer of information from an industrial control system network”

U.S. Patent # 8,938,795 “System for real-time cross-domain system packet filtering”

U.S. Patent # 8,898,227 “NFS storage via multiple one-way data links”

U.S. Patent # 8,887,276 “System for providing a secure video display”

U.S. Patent # 8,831,222 “Bilateral communication using multiple one-way data links”

U.S. Patent # 8,776,254 “System and method for the secure unidirectional transfer of software and software updates”

U.S. Patent # 8,732,453 “Secure acknowledgment device for one-way data transfer system”

U.S. Patent # 8,565,237 “Concurrent data transfer involving two or more transport layer protocols over a single one-way data link”

U.S. Patent # 8,498,206 “Secure one-way data transfer system using network interface circuitry”

U.S. Patent # 8,353,022 “Bilateral communication using multiple one-way data links”

U.S. Patent # 8,352,450 “Database update through a one-way data link”

U.S. Patent # 8,266,689 “Bilateral communication using multiple one-way data links”

U.S. Patent # 8,139,581 “Concurrent data transfer involving two or more transport layer protocols over a single one-way data link”

U.S. Patent # 8,068,415 “Secure one-way data transfer using communication interface circuitry”

U.S. Patent # 7,992,209 “Bilateral communication using multiple one-way data links”

U.S. Patent # 7,941,526 “Transmission of syslog messages over a one-way data link”

U.S. Patent # 7,675,867 “One-way data transfer system with built-in data verification mechanism”

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